

**FIG. 1**

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OP Code	Register #	Register #	Register #
Scalar-Vector Multiplication	Scalar Register	Source Vector Register	Destination Register

4                    5                    6                    7

00000000 00000000 00000000 00000000

**FIG. 2**

2

A <sub>0</sub>	A <sub>1</sub>	A <sub>2</sub>	...	A <sub>63</sub>
B <sub>0</sub>	B <sub>1</sub>	B <sub>2</sub>	...	B <sub>63</sub>
C <sub>0</sub>	C <sub>1</sub>	C <sub>2</sub>	...	C <sub>63</sub>
D <sub>0</sub>	D <sub>1</sub>	D <sub>2</sub>	...	D <sub>63</sub>
		• • •		

00000000000000000000000000000000

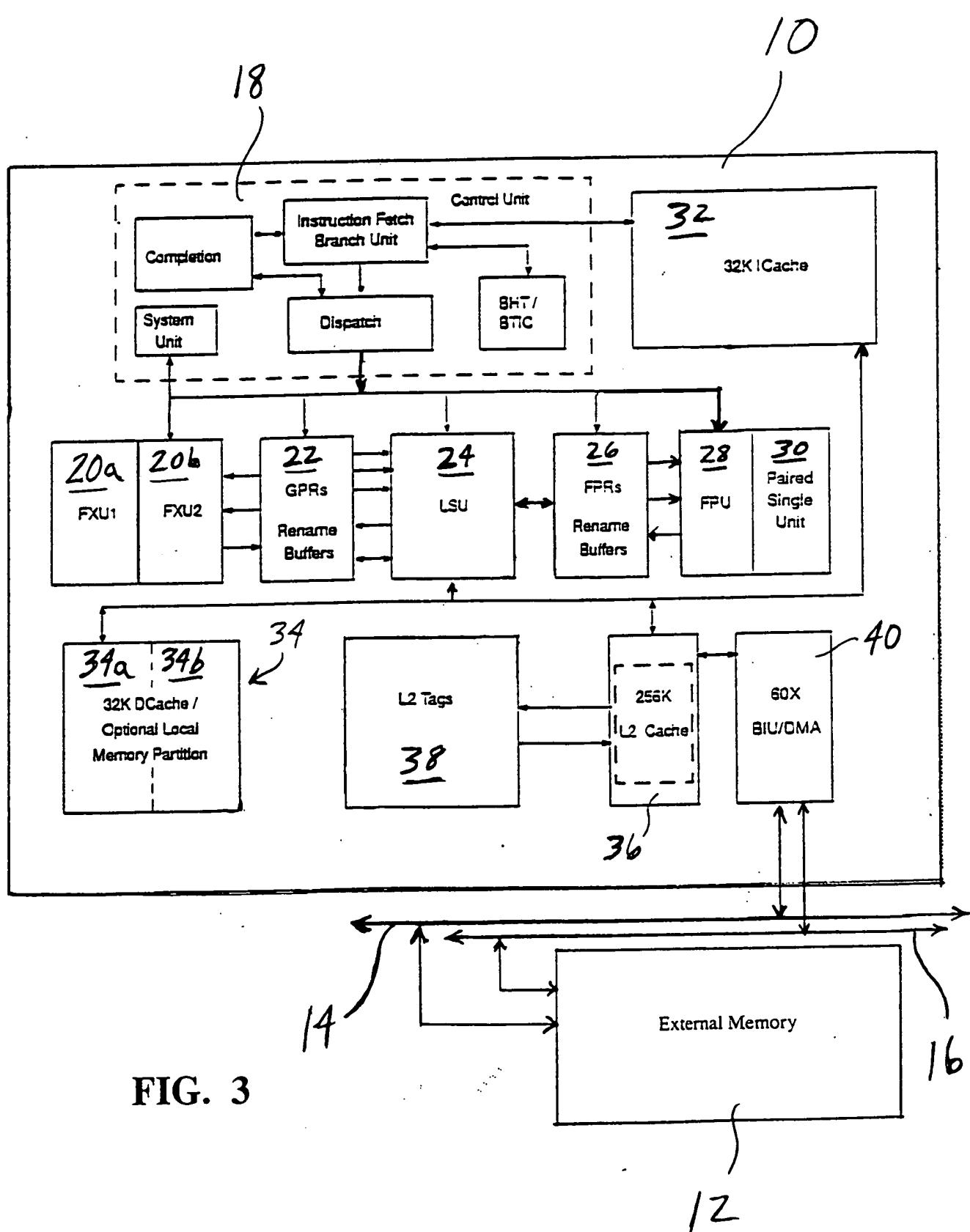


FIG. 3

### HID2 register bit settings

Bit(s)	Name	Description
0	LSQE	Load/Store quantized enable (non-indexed format) 0 psq_l[u] and psq_st[u] instructions are illegal 1 psq_l[u] and psq_st[u] instructions can be used
1	WBE	Write buffer enable 0 write buffer is disabled 1 write buffer enabled to gather non-cacheable data
2	PSE	Paired singles enabled 0 paired singles instructions are illegal 1 paired singles instructions can be used
3	LCE	Locked cache enable 0 Cache is not partitioned - 32 kB of normal cache 1 Cache is partitioned - 16 kB of normal cache and 16 kB of locked cache available
4-7	DMAQL	DMA queue length (read only) the number of used queue positions in the DMA, from 0 (queue empty) to 15 (queue full)
8-31	-	Reserved

FIG. 4

00100100 00100100 00100100 00100100

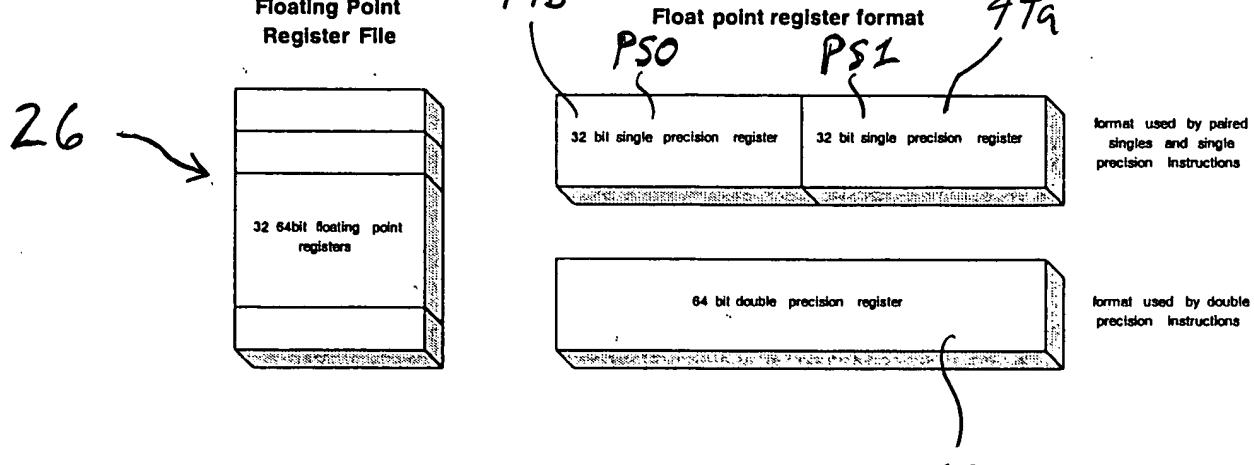


FIG. 5

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Op Code	Register #	N Position Bit(s)	Register #	Register #
Scalar-Vector Multiplication	Source Vector Register 1	Position Bit	Source Vector Register 2	Destination Vector Register

48      50      52      54      56

**FIG. 6**

00000000000000000000000000000000

### **ps\_addx**

Paired Single Add

**ps\_add**      frD, frA, frB      (Rc = 0)

**ps\_add.**      frD, frA, frB      (Rc = 1)

4	D	A	B	00000	21	Rc
0	5 6	10 11	15 16	20 21	25 26	30 31

**FIG. 7**

**ps\_madds0x**

Paired Single Multiply-Add Scalar High

**ps\_madds0**      **frD,frA,frC,frB**    (**Rc = 0**)

**ps\_madds0.**      **frD,frA,frC,frB**    (**Rc = 1**)

4	D	A	B	C	14	Rc
0	5 6	10 11	15 16	20 21	25 26	30 31

$$\text{frD\_ps0} = \text{frA\_ps0} * \text{frC\_ps0} + \text{frB\_ps0}$$

$$\text{frD\_ps1} = \text{frA\_ps1} * \text{frC\_ps0} + \text{frB\_ps1}$$

**FIG. 8**

**ps\_maddslx**

Paired Single Multiply-Add Scalar Low

**ps\_madds1**      **frD,frA,frC,frB**    (**Rc = 0**)

**ps\_madds1.**      **frD,frA,frC,frB**    (**Rc = 1**)

4	D	A	B	C	15	Rc
0	5 6	10 11	15 16	20 21	25 26	30 31

$$\text{frD\_ps0} = \text{frA\_ps0} * \text{frC\_ps1} + \text{frB\_ps0}$$

$$\text{frD\_ps1} = \text{frA\_ps1} * \text{frC\_ps1} + \text{frB\_ps1}$$

**FIG. 9**